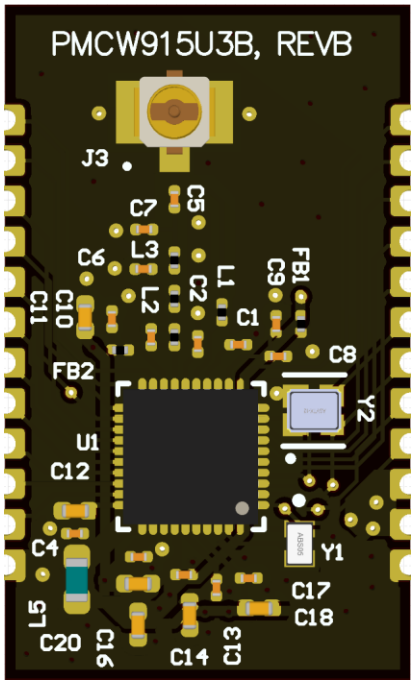
PMCW915U3B

915 MHz Wireless Sensor Gateway Module

Product Datasheet

Module revision B · Document issue 2.1 · May 2026 · Preliminary

Power Micro Controls



> **Engineering document.** The module is not certified in any country (see §11). Values shown as TBD still require bench characterization by customers.

1. Part number

```
PMC W 915 U 3 B
 |  |  |  | | |
 |  |  |  | | +---- Revision B
 |  |  |  | +------ 3.3 V supply
 |  |  |  +-------- UART host interface
 |  |  +----------- 915 MHz ISM band
 |  +-------------- Wireless
 +----------------- Power Micro Controls
```

Item	Value
Ordering part number	`PMCW915U3B`
Radio SoC	EFR32FG23A020F512GM40-B
Firmware	PMCW915U3B Radio Gateway, v2.1.0
Host protocol	UART protocol 1.3.0
Host interface	2 × UART (3.3 V logic), SWD debug
Supply	3.3 V nominal (`BAT+`)

2. Description

PMCW915U3B is a 915 MHz sub-GHz radio module that retrieves biometric sensor data (PPG optical and EDA electrodermal) from wrist-worn sensor nodes and delivers it to a host processor over UART.

The module arrives with its firmware already loaded and ready to run. Every function is reachable through a documented UART interface: identifying the module, configuring the radio, polling a sensor, retrieving stored data, persisting settings and, in a future release, updating firmware. The interface was shaped around the way a host application actually uses the radio, so a working integration is a short job rather than a project. The module owns the certified radio PHY, the over-the-air command grammar and a non-volatile configuration store; the host owns everything else.

The radio operates strictly in poll/response. Sensor nodes never transmit unsolicited, so all channel traffic is initiated and rate-controlled by the host. That property is what keeps dense deployments manageable, with hundreds of wearables per site and overlapping modules for redundancy.

2.1 Key features

- 915 MHz ISM band, 26 channels (902 to 927 MHz on 1 MHz spacing), 2-GFSK at 50 kbps
- Up to +20 dBm conducted output, with the ceiling enforced in firmware
- Certified envelope enforced in firmware. No host command can operate the radio outside its channel plan or power grant, and out-of-range values are rejected without ever being applied or stored
- Stateless sensor addressing. Sensors are addressed by inline 64-bit EUI, so one module serves an unlimited number of enrolled wearables and pairing stays entirely a host concern
- Promiscuous receive forwarding. The module reports every valid sensor frame it demodulates, including replies to polls issued by other modules, which is what allows multi-module redundancy with host-side de-duplication
- Two UART grammars: a framed binary machine API and a human-readable text console
- Twelve host-controllable GPIOs on the module headers, driven and sensed over the same UART protocol. Six modes per pin, atomic multi-pin writes, edge-change indications and a persisted power-on state. Pins are addressed by logical index, so the pins the module reserves for itself are unreachable by any host command
- Non-volatile configuration that survives power cycles and firmware updates

- Single 3.3 V supply, internal DC-DC, 32.768 kHz and 39 MHz references on-module
- Firmware pre-loaded at the factory, supplied with a generated C header and a documented UART API built for straightforward integration

3. Block diagram

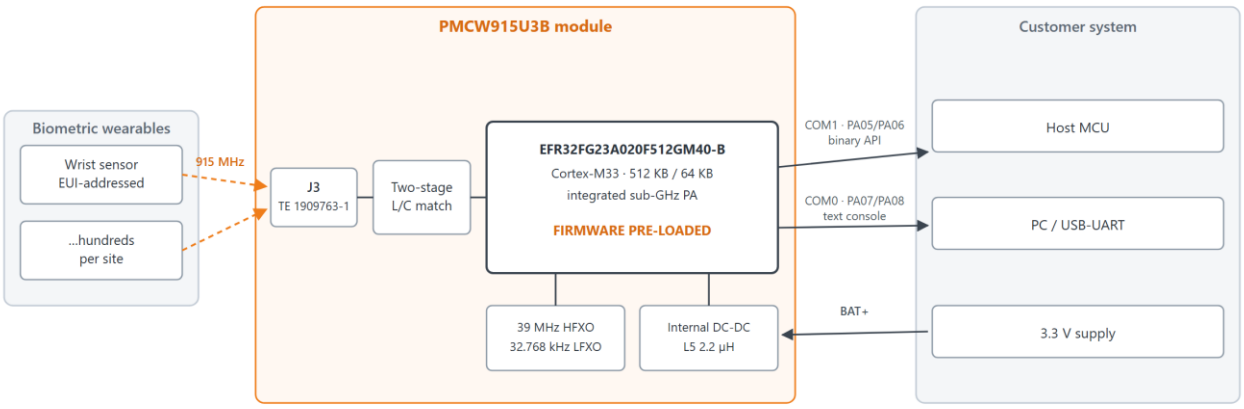


Figure 1 — PMCW915U3B block diagram

4. Pin descriptions

The module presents its host interface on two 12-pin castellations.

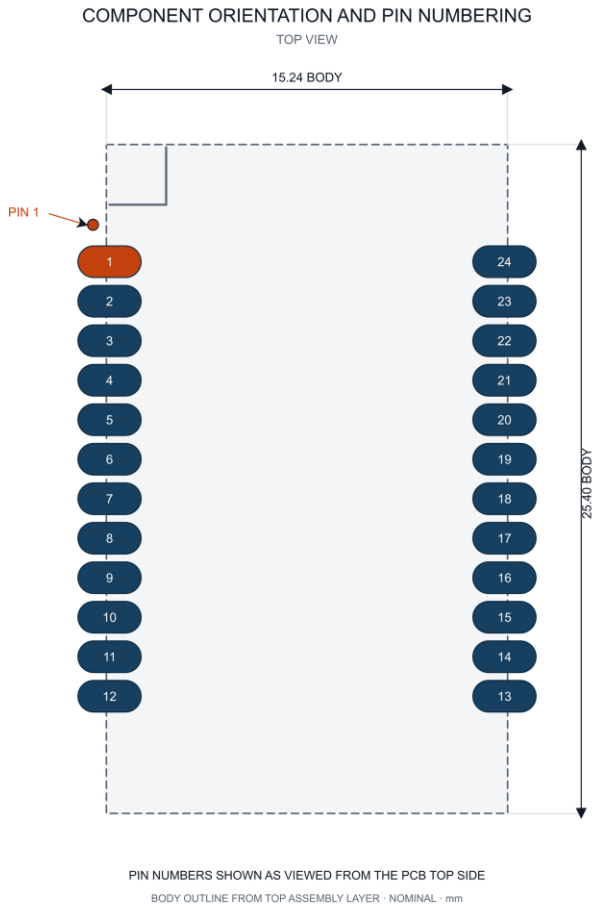


Figure 1. Pin Diagram

4.1 Row 1 — control, UART, debug

Pin	Signal	SoC pin	Type	Description
1	PB01	PB01	I/O	GPIO 0. Host-controllable general-purpose I/O. See §10.3.
2	PB00	PB00	I/O	GPIO 1. Host-controllable general-purpose I/O. See §10.3.
3	PA00	PA00	I/O	GPIO 2. Host-controllable general-purpose I/O. See §10.3.
4	SWCLK	PA01	In	Serial-wire debug clock. Factory and service use.
5	SWDIO	PA02	I/O	Serial-wire debug data. Factory and service use.
6	SWO/SWV	PA03	Out	Serial-wire trace output. Factory and service use.
7	PA04	PA04	I/O	GPIO 3. Host-controllable general-purpose I/O. See §10.3.
8	COM1_TX	PA05	Out, 3.3 V	Binary host API, module transmit. Connect to host RX.
9	COM1_RX	PA06	In, 3.3 V	Binary host API, module receive. Connect to host TX.
10	COM0_TX	PA07	Out, 3.3 V	Text console, module transmit.
11	COM0_RX	PA08	In, 3.3 V	Text console, module receive.
12	GND	—	Power	Ground.

4.2 Row 2 — reset, GPIO, power

Pin	Signal	SoC pin	Type	Description
1	`RESET`	RESET	In, active low	Module reset. Drive low for at least 10 µs to reset; leave open or high for normal operation. Internally pulled up.
2	`PC07`	PC07	I/O	GPIO 11. Host-controllable general-purpose I/O. See §10.3.
3	`PC06`	PC06	I/O	GPIO 10. Host-controllable general-purpose I/O. See §10.3.
4	`PC05`	PC05	I/O	GPIO 9. Host-controllable general-purpose I/O. See §10.3.
5	`PC04`	PC04	I/O	GPIO 8. Host-controllable general-purpose I/O. See §10.3.
6	`PC03`	PC03	I/O	GPIO 7. Host-controllable general-purpose I/O. See §10.3.
7	`PC02`	PC02	I/O	GPIO 6. Host-controllable general-purpose I/O. See §10.3.
8	`PC01`	PC01	I/O	GPIO 5. Host-controllable general-purpose I/O. See §10.3.
9	`PC00`	PC00	I/O	GPIO 4. Host-controllable general-purpose I/O. See §10.3.
10	`BAT+`	—	Power in	3.3 V supply. Tie pins 10 and 11 together at the source.
11	`BAT+`	—	Power in	3.3 V supply.
12	`GND`	—	Power	Ground.

> **The twelve pins marked `GPIO n` are customizable.** They are default hi-Z (mode 0, disabled), so an unconfigured module never drives a customer net and a floating GPIO reads as undefined until you configure it. A pin only drives, or only applies a pull-up or pull-down, once its mode has been set. Set it live with `GPIO_CONFIG`, or persistently by staging `gpio_mode` and `gpio_out_default` with `CFG_SET` and issuing `CFG_COMMIT`. Committed settings are re-applied at every power-on, so the power-on state of every net you connect is deterministic and chosen by you. See §10.3.
>
> **Pin safety.** The pins the module reserves for itself are not addressable by any host command: `COM1` (PA05/PA06), `COM0` (PA07/PA08), the debug port (PA01/PA02/PA03) and the internal PA/LNA control lines (PD02/PD03). The wire protocol identifies a pin only by its logical index 0 to 11, and the index table contains nothing but the twelve header GPIOs above. No opcode or parameter accepts a raw SoC port and pin, so no command sequence can repurpose a UART, debug or PA control pin.

Minimum connection for operation: `BAT+` (both pins), `GND` (both headers) and one UART pair. Use `COM1_TX`/`COM1_RX` for machine integration or `COM0_TX`/`COM0_RX` for console use. `RESET` is recommended so the host can recover the module unconditionally.

4.3 RF connector

Reference	Part	Description
J3	TE Connectivity 1909763-1	50 Ω RF output. Connect a matched 915 MHz antenna or a 50 Ω instrument.

> **Never transmit without a load on J3.** Operating the PA into an open or a short can damage the output stage.

5. Absolute maximum ratings

Stresses beyond these limits may cause permanent damage. These are stress ratings only; functional operation is not implied.

Symbol	Parameter	Min	Max	Unit	Note
V_BAT	Supply voltage at `BAT+`	−0.3	3.8	V	Per SoC vendor limit
V_IO	Voltage on any I/O pin	−0.3	V_BAT + 0.3	V	Not 5 V tolerant. See §12.2
I_IO	Current into/out of any I/O pin	—	TBD	mA	
P_RF	RF power into J3	—	TBD	dBm	Receiver survivability to be characterized
T_STG	Storage temperature	TBD	TBD	°C	
ESD	Human body model	—	TBD	kV	No dedicated I/O ESD protection on the module. See §12.3

6. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_BAT	Supply voltage (`BAT+`)	TBD	3.3	TBD	V
V_IH	UART input high	0.7 × V_BAT	—	V_BAT	V
V_IL	UART input low	0	—	0.3 × V_BAT	V
T_A	Ambient operating temperature	TBD	25	TBD	°C
Z_ANT	Antenna impedance at J3	—	50	—	Ω

The module regulates internally from `BAT+` using the SoC's DC-DC converter (2.2 µH inductor on VREGSW), with ferrite-isolated supply domains for the RF and PA rails (33 Ω bead on the PA rail, 70 Ω bead on the DC-DC rail).

Supply design guidance. Size the 3.3 V source for the transmit burst current (§7, still TBD) plus margin. Transmit bursts last ≈337 ms (§9) and draw substantially more than the receive-idle current, so a supply that sags under pulsed load will cause transmission failures that look like intermittent radio problems.

7. Electrical characteristics

Every value in this section requires bench characterization. They are listed to define the measurement plan, not to specify the module.

Symbol	Parameter	Conditions	Value	Unit
I_RX	Supply current, receive idle	3.3 V, listening	TBD	mA
I_TX20	Supply current, transmitting	3.3 V, +20 dBm	TBD	mA
I_TX0	Supply current, transmitting	3.3 V, 0 dBm	TBD	mA
I_AVG	Average current, one poll per minute	3.3 V, +20 dBm	TBD	mA
I_INRUSH	Peak inrush at power-up	Cold start	TBD	mA
I_OH / I_OL	GPIO output drive current, per pin	3.3 V, push-pull	TBD	mA
V_OL	GPIO output low voltage	3.3 V, at rated I_OL	TBD	V
V_OH	GPIO output high voltage	3.3 V, at rated I_OH	TBD	V
I_LEAK	GPIO input leakage current	3.3 V, mode 1 (input), pin at rail	TBD	µA

Characterization plan. Measure at `BAT+` during (a) receive idle, (b) a 2096-byte transmit burst at +20 dBm and at 0 dBm, (c) a sustained poll cycle at one transaction per second, and (d) power-up inrush. Because the duty cycle in a polled deployment is low, average current is expected to be dominated by receive idle, so quantify both.

GPIO characterization plan. For the header GPIOs (§10.3), measure per-pin sink and source current at the SoC's selected drive strength, `V_OL` and `V_OH` at that current, and input leakage in plain-input mode with the pin tied to each rail. Also record the total current permitted across all twelve pins simultaneously and the pull-up/pull-down resistor value in modes 2 and 3. Neither figure is specified until it has been measured. Do not design a load around these pins until this block is characterized; the absolute-maximum I_IO limit in §5 is itself still TBD.

8. RF characteristics

The PHY is fixed and certification-frozen. No host command can alter it.

Parameter	Value	Note
PHY identifier	`PHY_Studio_915M_2GFSK_50Kbps_25K`	Reported by `MOD_INFO`
Modulation	2-GFSK	
Base frequency	902.000 MHz	Channel 0
Channel spacing	1.000 MHz	
Channel plan	0 … 25 (902 – 927 MHz)	Firmware-clamped; `ERR_CERT_LIMIT` beyond
Data rate	50 kbps	
Deviation	25 kHz	
Sync word	0xF68D (16-bit)	
Preamble	40 bits	
CRC	Hardware, enabled	Failing frames silently discarded
Whitening	Disabled	
Frame length	Fixed, 2096 bytes	Both directions; read-only parameter `frame_size`
Max conducted TX power	+20.0 dBm (200 deci-dBm)	Firmware ceiling
Min TX power setting	−10.0 dBm (−100 deci-dBm)	
Reference oscillator	39 MHz	On-module
RX sensitivity	TBD	Expect roughly −107 dBm at 50 kbps; must be measured
Range	TBD	Site- and antenna-dependent
Harmonics / spurious	TBD	Required for certification

8.1 Fixed-length framing consequence

Every on-air transaction occupies a full 2096-byte frame, whether it carries a 48-byte command or a 2048-byte data page. This is a certification-frozen property with direct consequences for capacity (§9), and configuration cannot change it.

9. Timing and capacity

Derived from the PHY and verified on hardware.

Parameter	Value	Derivation
Frame airtime	≈337 ms	2096 B × 8 / 50 kbps, plus preamble/sync/CRC
Poll transaction (command + reply)	≈0.7 s	Two frames plus turnaround
Channel throughput	≈1.3–1.4 transactions/s	One outstanding request at a time
Sensor status poll	≈0.7 s of airtime	One transaction
Full event retrieval (64 pages)	≈45–50 s	64 transactions

Deployment budget (one channel, shared by every module within range):

Scenario	Airtime	Channel duty
100 wearables, status poll every 6 h	70 s per 6 h	≈0.3 %
300 wearables, status poll every 1 h	3.5 min per h	≈6 %
Continuous event retrieval	≈1 event per minute	≈75 %

Status polling is nearly free. Event retrieval is the scarce resource and has to be scheduled by the host. Sites needing more capacity can partition wearables and modules across the 26 available channels.

10. Host interface summary

Port	SoC pins	Header 1 pins	Baud	Role
COM1	PA05 (TX) / PA06 (RX)	8, 9	460800 8N1	Machine API. Framed binary protocol, version-frozen contract.
COM0	PA07 (TX) / PA08 (RX)	10, 11	460800 8N1	Text console, plus binary (auto-detected on `0xA5`). Convenience grammar.

Both ports operate at 3.3 V logic levels with no hardware flow control. Complete protocol and command documentation is in the PMCW915U3B User Manual.

10.1 Configuration parameters

Seventeen parameters, persisted in non-volatile memory and applied live on commit. Certification-bound parameters are validated against compile-time hard caps.

ID	Parameter	Range	Default	Cert-bound
0x0001	`role`	0–1	1	—
0x0002	`operating_channel`	0–25	10	Yes
0x0003	`tx_power_ddbm`	−100 … 200	200	Yes
0x0010	`rx_forward_enable`	0–1	1	—
0x0011	`decode_records`	0–1	1	—
0x0020	`tx_delay_ms`	0–65535	500	—
0x0021	`tx_timeout_ms`	0–65535	7000	—
0x0022	`no_response_retries`	0–65535	5	—
0x0040	`hop_enable`	0–1	1	—
0x0041	`hop_table_len`	0–25	25	Yes
0x0042	`hop_table`	25 × ch 0–25	zeros	Yes
0x0043	`hop_dwell_ms`	0–65535	400	Yes
0x0050	`gpio_mode`	12 × mode 0–5	zeros (all hi-Z)	—
0x0051	`gpio_out_default`	bitmask 0–4095	0	—
0x0052	`gpio_irq_mask`	bitmask 0–4095	0	—
0x00F0	`frame_size`	2096 (read-only)	2096	Yes
0x00F1	`local_eui`	16 ASCII hex (read-only)	device unique ID	—

The four `hop_*` parameters do not switch hopping on. They are accepted, validated and persisted, but the hop engine is dormant in this firmware and the radio stays on `operating_channel`. `hop_enable` ships set to 1 and `MOD_STATUS` echoes that value, so neither the parameter nor the status field indicates that hopping is running (§11). Channel selection and any site-level channel plan are host responsibilities.

10.2 Biometric Sensor data

Each data reply carries a 2048-byte sensor page holding 45 records of 45 bytes, so 2025 bytes are used and 23 are spare. One sensor event is 64 pages, roughly 3 minutes of sensing.

Offset	Size	Field	Endianness	Conversion
0	4	Timestamp (sensor tick counter)	Big	Raw ticks, not wall-clock
4	1	Millisecond counter (0–15)	—	Raw
5	12	PPG green / red / IR / dark	24-bit MSB-first	Raw ADC counts
17	12	EDA A-I, A-Q, B-I, B-Q	24-bit MSB-first	Raw counts
29	2	Object temperature	Little (int16)	°C = raw / 100
31	6	Accelerometer X/Y/Z (±2 g)	Little (int16)	mg = raw × 0.061
37	6	Gyroscope X/Y/Z (±2000 dps)	Little (int16)	mdps = raw × 70
43	2	IMU die temperature	Little (int16)	°C = raw / 256 + 25

Nominal sensor rates: PPG ≈16 Hz, EDA ≈4 Hz. The 24-bit byte order is MSB-first pending confirmation against instrumented sensor hardware.

10.3 General-purpose I/O

Twelve header pins are available to the host as general-purpose I/O over the same UART interface used for everything else. Pins are addressed by logical index only. The protocol has no concept of a SoC port and pin, which is what keeps the module's own pins out of reach (see the pin-safety note in §4).

GPIO index	SoC pin	Header	Header pin
0	PB01	1	1
1	PB00	1	2
2	PA00	1	3
3	PA04	1	7
4	PC00	2	9
5	PC01	2	8
6	PC02	2	7
7	PC03	2	6
8	PC04	2	5
9	PC05	2	4
10	PC06	2	3
11	PC07	2	2

Each pin takes one of six modes:

Mode	Meaning
0	Disabled. Hi-Z, no pull. Factory default on every pin.
1	Input, no pull
2	Input with pull-up
3	Input with pull-down
4	Output, push-pull
5	Output, open-drain

Operations are `GPIO_CONFIG` (mode + initial level), `GPIO_WRITE` and `GPIO_READ` for a single pin, `GPIO_WRITE_MASK` for an atomic multi-pin write, `GPIO_READ_ALL` for a snapshot of all twelve, and the asynchronous `GPIO_CHANGE_IND` for edge notification on input pins selected by `gpio_irq_mask`. An operation that does not match the pin's current mode returns `ERR_PIN_MODE` (`0x0050`); writing a pin configured as an input is the usual case.

`GPIO_CONFIG` applies immediately but is not persistent. To fix the power-on state of a net, stage `gpio_mode` and `gpio_out_default` with `CFG_SET` and commit them. The module re-applies both before the host has a chance to issue any command after reset.

Electrical limits for these pins are not yet characterized (§7). Complete opcode payload definitions, console commands and worked examples are in the PMCW915U3B User Manual.

11. Regulatory status

> **This module has not yet been granted certification in any country. Product certification is the responsibility of the end customer.** Present use is limited to engineering evaluation.

Item	Status
FCC Part 15.247 modular grant (USA)	Planned, not started
Certified envelope (design target)	902–927 MHz, 26 channels, ≤ +20 dBm conducted
Firmware envelope enforcement	Implemented and verified. An out-of-range channel or power value returns `ERR_CERT_LIMIT`, is never applied and is never stored
Frequency hopping	Parameters present and persisted, hop engine dormant in v2.1.0. `hop_enable` ships set to 1 without hopping being active (§10.1). Certify the mode actually shipped, which today is a single-channel radio.
Antenna	Final antenna and connector treatment (unique-connector versus listed-antenna) to be determined with the test lab
Emissions, band edge, PSD, harmonics	Not yet measured

Integrator obligation. A modular grant constrains the antennas that may be used and requires specific host-product labelling. Do not ship an end product containing this module until the grant exists and its conditions are known.

12. Integration guidance

12.1 Typical connection

Module signal	Connect to
`COM1_TX` / `COM1_RX` (H1-8 / H1-9)	Host MCU UART, the production control path
`COM0_TX` / `COM0_RX` (H1-10 / H1-11)	3.3 V USB-UART bridge for bench work, diagnostics and field service
`RESET` (H2-1)	Host GPIO (open-drain preferred), so the host can force a known state
`GPIO 0…11` (H1-1/2/3/7, H2-2…H2-9)	Optional. Carrier-board nets you want the host to drive or sense through the module (§10.3). Unused GPIOs may be left unconnected.
`BAT+` (H2-10, H2-11)	3.3 V rail, both pins
`GND` (H1-12, H2-12)	Ground plane, both pins
`J3`	50 Ω antenna

Exposing the console port to a USB-UART bridge on the carrier board is strongly recommended. It gives field technicians a human-readable diagnostic interface with no custom software.

12.2 Logic levels

Module I/O runs at 3.3 V and is not 5 V tolerant. Level-shift any 5 V host. Ensure the host's UART idles high before the module leaves reset, so the first byte is not framed as a break condition.

12.3 Layout and EMC

- Keep the J3 antenna trace at 50 Ω, short, and clear of digital switching.
- Provide continuous ground under the module, with vias on both `GND` pins.
- Decouple the 3.3 V rail close to `BAT+`. The module supplies its own local decoupling and ferrite isolation, but pulsed PA current must be sourced by the carrier board.

- The module does not include dedicated ESD protection on the UART or debug pins. Add protection on any signal routed to an external connector.

12.4 Debug port

`SWCLK`, `SWDIO`, and `SWO` are exposed for factory programming and service. They are not part of the host interface. Production units are intended to ship debug-locked (§13), so plan any board-level access accordingly.

13. Security and field update

Item	Status
Firmware delivery	Pre-loaded at the factory and ready to run, supplied with the generated protocol header and full API documentation
Configuration authority	Host-controlled over UART, with state held in on-module non-volatile memory
Firmware update method	Physical connection to the debug port (`SWCLK` / `SWDIO` / `SWO`, §12.4). The module carries no bootloader and accepts firmware neither over UART nor over the air.
Field firmware update (`FW_UPDATE_ENTER`)	Reserved, and not planned for this module. The opcode returns `ERR_STATE` for **any** key and does not reboot; the unlock key is not checked, so a rejection is not an authentication result.
Signed / encrypted update images	Not applicable. Images are loaded by physical connection under factory or service control, not delivered by the host.
Debug lock / secure boot	Not yet applied. Production units must be debug-locked before shipment.
Service and update path on a locked unit	**Debug unlock-with-erase.** Unlocking a production unit erases it, so a field update is always a full reprogram. The module boots by default to **channel 10, +20.0 dBm** with NVM3 cleared, so every unit must be re-provisioned (channel, TX power, GPIO power-on state) after service.

14. Mechanical

Item	Value
Module outline	TBD
Header type and pitch	2 × 12-pin, pitch TBD
Height above carrier board	TBD
Mass	TBD
Mounting	TBD
Moisture sensitivity level	TBD

A dimensioned mechanical drawing and a recommended carrier-board footprint must accompany the released datasheet.

15. Revision history

Issue	Date	Change
1.0	March 2023	First issue.
1.1	February 2024	Revised for the current module hardware.
2.0	November 2025	Host interface and configuration sections reworked.
2.1	May 2026	Current issue. Firmware v2.1.0 and protocol 1.3.0: stateless EUI addressing, dual UART grammars, non-volatile configuration, twelve host-controllable GPIOs, and certification-envelope enforcement.

16. Landing Pattern

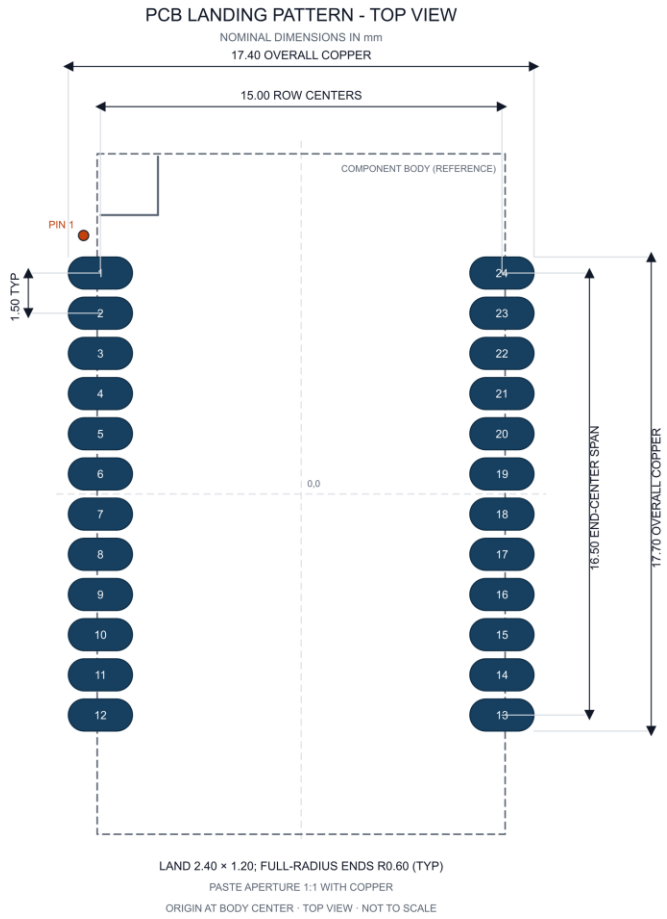


Figure 2. PCB Landing Pattern

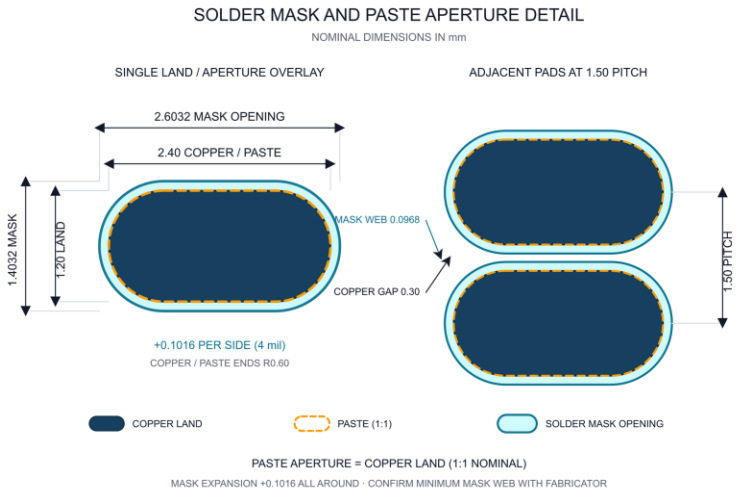


Figure 3. Solder Masking